

REMARKS

Claims 1-19 are pending in the application. Claims 14-19 are added via the present Amendment.

35 U.S.C. § 102:

Claims 1, 3-5, 7, 9 and 10 are rejected under 35 U.S.C. § 102(b) as being anticipated by Shirley, et al. (U.S. Patent No. 6,015,729 [hereinafter “Shirley”]).

Applicant thanks the Examiner for the courtesies extended during the interview of February 8, 2007, where the present rejection was discussed. The Examiner asserts that the decoupling capacitor is formed by the area immediately between the overlapping areas of elements 28 and 24 in Figure 1 of Shirley.

As noted during the interview, a difference between an exemplary embodiment of the present invention and Shirley is that the present electrode comprising the shield layer is extended into the decoupling capacitor while being in the same plane as the plane shape portion that contacts the diffusion layer. Shirley does not disclose at least this feature. As shown in Figure 1 of Shirley, the portion of element 28 that contacts element 16 is applied against the claimed plane shaped portion of the shield layer that contacts the diffusion layer. However, the plane shaped portion of 28, which contacts element 16, is not extended into the decoupling capacitor while remaining in the same plane.

Accordingly, Applicant respectfully submits that claims 1 and 3 are not anticipated by Shirley, such that the rejection under 35 U.S.C. § 102(b) should be withdrawn. The rejection of dependent claims 4, 5, 7, 9 and 10 should likewise be withdrawn at least by virtue of their respective dependencies upon claims 1 and 3.

35 USC § 103:

Claims 2, 6, 8, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirley in view of Tobita (U.S. patent No. 5,801,412).

The Examiner acknowledges that Shirley does not explicitly teach or suggest the features of claim 2 regarding a wiring layer connected to wirings on an uppermost layer of a multi-layer wiring structure via contact electrodes, and a capacitor insulating film for forming the decoupling capacitor provided between the wiring layer and the shield layer. Shirley also does not teach that the shield layer comprises a silicon compound of a metal. Therefore, the Examiner relies on Tobita. Applicant respectfully submits that Tobita fails to make up for the deficient teachings of Shirley in regard to claims 1 and 3, such that claims 2, 6, 8, 11 and 12 are patentable at least due to their respective dependencies.

NEW CLAIMS:

Applicant adds new claims 14-19 to obtain more varied protection for the present invention. Applicant respectfully submits that claim 14 is deemed patentable over the applied references. For example, claim 14 describes that a plane shaped portion of the shield layer contacts the diffusion layer and is a lowermost conductive layer on the semiconductor substrate. Applicant submits that the applied references do not disclose the unique combination of features in claim 14, including the recited shield layer. Claims 15-19 are deemed patentable over the prior art at least by virtue of their respective dependencies upon claim 14 in addition to their individual recitations.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

AMENDMENT UNDER 37 C.F.R. § 1.111
U.S. Patent Application No. 10/669,655

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Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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